

In the Claims:

Please amend the claims 1-5, 7-13, and 16-20 as follows:

1. (Currently amended) A chip separation method comprising:

providing a wafer comprising a chip, the chip comprising a close-loop boundary line consisting of N straight-line chip boundary lines shared with N other chips on the wafer, N being a positive integer greater than 2; and

cutting around the chip along M straight-line cut segments on the chip, M being a positive integer, wherein M > N. A method for cutting a chip from a wafer, the method comprising the step of cutting around the chip along a plurality of straight-line cut segments such that all resulting corners of the chip after cutting have an angle greater than 90°.

2. (Currently amended) The method of claim 1, wherein the angles of all the resulting corners of the chip after cutting are equal, wherein each corner of the corners of the chip after cutting is defined by two consecutive straight-line cut segments of the M straight-line cut segments.

3. (Currently amended) The method of claim 1, wherein at least two consecutive straight-line cut segments of the plurality of M straight-line cut segments which are not on any the N straight-line chip boundary lines are of thea same length.

4. (Currently amended) The method of claim 1, wherein all the straight-line cut segments of the plurality of M straight-line cut segments which are not on any the N straight-line chip boundary lines are of thea same length.

5. (Currently amended) The method of claim 1, wherein ~~the step of said~~ cutting around the chip along the plurality of M straight-line cut segments comprises the steps of:

cutting, with a laser beam, along the straight-line cut segments of the plurality of M straight-line cut segments which are not on any the N straight-line chip boundary lines, and
cutting, with a saw blade, along the straight-line cut segments of the plurality of M straight-line cut segments which are on the N straight-line chip boundary lines of the chip.

6. (Original) The method of claim 1, wherein the cutting goes as deep as the entire thickness of the chip along the plurality of straight-line cut segments.

7. (Currently amended) The method of claim 1, wherein the cutting goes as deep as the entire thickness of the chip along the straight-line cut segments of the plurality of M straight-line cut segments which are on the N straight-line chip boundary lines of the chip, and wherein the cutting goes only as deep as a Back End Of Line (BEOL) BEOL layer along the straight-line cut segments of the plurality of M straight-line cut segments which are not on any chip boundary line.

8. (Currently amended) The method of claim 1, wherein cutting along the straight-line cut segments of the plurality of M straight-line cut segments which are not on the N straight-line chip boundary lines of the chip are performed with a laser beam and as deep as a Back End Of Line (BEOL) layer of the chip, and wherein cutting along the straight-line cut segments of the plurality of M straight-line cut segments which are on the N straight-line chip boundary lines of the chip are performed with a saw blade and as deep as entire the thickness of the chip.

9. (Currently amended) A semiconductor wafer comprising a chip, the chip comprising a close-loop boundary line consisting of N straight-line chip boundary lines shared with N other chips of the wafer, N being a positive integer greater than 2, the chip further comprising cuts along M straight-line cut segments, M being a positive integer, wherein $M > N$. A semiconductor chip structure, comprising a plurality of straight-line cut segments around the chip such that all angles of corners of the chip are greater than 90° .

10. (Currently amended) The wafer chip structure of claim 9, wherein the angles of all the corners of the chip are equal, wherein each corner of the corners of the chip is defined by two consecutive straight-line cut segments of the M straight-line cut segments.

11. (Currently amended) The wafer chip structure of claim 9, wherein at least two consecutive straight-line cut segments of the M plurality of straight-line cut segments which are not on the N straight-line chip boundary lines of the chip before dicing are of the same length.

12. (Currently amended) The wafer chip structure of claim 9, further comprising a Back End of Line (BEOL) layer which comprises a low-K material, wherein the BEOL layer resides at a top surface of the wafer.

13. (Currently amended) A chip separation method comprising:
providing a wafer comprising a plurality of chips sharing straight-line chip boundary lines; and

for each chip of the plurality of chips having a close-loop boundary line consisting of N straight-line chip boundary lines, N being an integer greater than 2, cutting around the chip along M straight-line cut segments on the chip, wherein M is an integer and M > N. A method of dieing, comprising the steps of:

— providing a wafer comprising a plurality of chips sharing chip boundary lines, and
— for each chip of the plurality of chips, cutting around the chip along a plurality of straight-line cut segments such that resulting corners of the chip after cutting are all greater than 90°.

14. (Original) The method of claim 13, wherein the cutting of one chip of the plurality of chips is finished before the cutting of another chip of the plurality of chips is started.

15. (Original) The method of claim 13, wherein the cutting of one chip of the plurality of chips is started before the cutting of another chip of the plurality of chips is finished.

16. (Currently amended) The method of claim 13, wherein the cutting is performed with a laser beam for straight-line cut segments of the plurality of straight-line cut segments which are not on any straight-line chip boundary line, and wherein the cutting is performed with a saw blade for all straight-line chip boundary lines comprising straight-line cut segments of the plurality of straight-line cut segments.

17. (Currently amended) The method of claim 13, wherein for straight-line cut segments of the plurality of straight-line cut segments which are not on the straight-line chip boundary lines, the cutting is only as deep as a Back End of Line (BEOL) layer, and wherein for straight-line cut segments of the plurality of straight-line cut segments which are on the straight-line chip boundary lines, the cutting is as deep as the entire thickness of the wafer.

18. (Currently amended) The method of claim 17, further comprising the step of cutting as deep as the entire thickness of the wafer along all the straight-line chip boundary lines.

19. (Currently amended) The method of claim 13, wherein the plurality of chips are arranged in rows and columns, and wherein at least one straight-line chip boundary line goes through at least two straight-line cut segments of at least two chips of the plurality of chips.

20. (Currently amended) The method of claim 13, wherein the straight-line cut segments of the plurality of straight-line cut segments which are not on any straight-line chip boundary line of the chip are of the same length.